Electronic Version
Stylesheet Version v1.1.1

FINFET SRAM CELL WITH CHEVRON FIN-FET LOGIC

Abstract

A electronic device, and SRAM and a method of forming the electronic device and SRAM. The semiconductor device including: a pass gate transistor having a fin body having opposing sidewalls aligned in a first direction and having a first majority carrier mobility and a gate adjacent to both sidewalls of the fin body; a pull down latch transistor having a fin body having opposing sidewalls aligned in a first direction and having a first majority carrier mobility and a gate adjacent to both sidewalls of the fin body; a pull up latch transistor having a fin body having opposing sidewalls aligned in a first direction and having a first majority carrier mobility and a gate adjacent to both sidewalls of the fin body; and CMOS chevron logic circuits, wherein crystal planes of each fin body and of CMOS transistor of the chevron logic are co-aligned.